

CECS 561 Spring 2018

Basic System

By

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04/06/2018

An audio recorder was built on the Zybo board using a new I2S IP.

# Introduction

An audio recorder was built on the Zybo board using a new I2S IP. This new IP (called LogicBricks LOGII2S) is available from Xylon through Vivado’s IP catalog. A free evaluation license can be obtained from the vendor’s website. The LOGII2S IP allows for 8x Rx/Tx channels to be configured for recording/playback on external audio hardware (i.e. the Zybo’s SSM2603 audio codec) via the I2S protocol.

# Operation

When a button is pressed, the Zynq board will record audio data from a microphone. When the button is released the audio-data will be played from a connected speaker.

# Theory

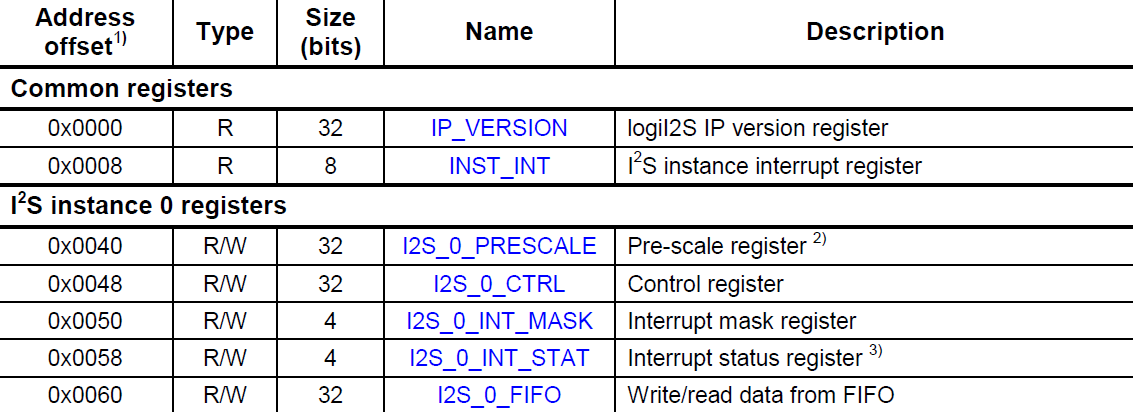
The LOGII2S IP is configured to have 1 receive channel and 1 transmit channel. Each of these channels has registers associated with it as shown in Figure 1.

Figure 1 The LOGII2S's register map. The table is taken from Xylon's documentation.

The LOGII2S IP uses interrupts to inform the system about the state of its registers. Interrupts can be configured to occur when a channel’s FIFO is empty, almost empty (user defined), almost full (user defined), and full. When any channel raises an interrupt

the INST\_INT register can be read to determine the source. The indicated channel’s I2S\_n\_INT\_STAT register can be read to determine which of the four interrupt types caused the event. The I2S\_n\_INT\_STAT register is also used to clear a given interrupt by writing a ‘1’ to any given position. The I2S\_n\_INT\_MASK register can be used to enable/disable the four interrupt conditions.

The I2S\_n\_PRESCALE value can be used to set the bit clock relative to the system clock. For example, if the system clock is 100 MHz then a pre-scale value of 4 would result in a bit clock value of 100 MHz / (2 \* 4) = 12.5 MHz. The factor of 2 is included for the case of stereo transmission, indicating that each channel was operate at an interleaved bit rate of 12.5 MHz.

I2S\_n\_CTRL register is used to enable/disable serial data transfers, and configure the values of the word select clocks among other functions minor functions.

The I2S protocol—Inter-IC Sound—uses 1+ data lines, 1 word select clock, and 1 bit clock. The word select clock is used to alternate between the L/R channels for stereo playback. For transmission, when the output is a stereo line, the data line consists of interleaved L/R samples as indicated by the word select clock with a serial data rate indicated by the bit clock.

# Hardware Design

Figure 2 The hardware platform for the basic system. It is the same as Lab 2 with the addition of the I2C interface and the LOGII2S IP.

The hardware platform is the same as Lab 2 with the addition of an I2C interface on the PS, the LOGII2S IP, and an additional AXI GPIO used for the digital mute control on the audio codec. The buttons IP from Lab 2 is used to control audio recording/playback.

# Software Design

Before using the Zybo’s audio codec it must be configured over I2C. The I2C functionality is enabled in the PS and accessed through the system software. The necessary configuration values are available in the SSM2603’s datasheet. The I2S IP is configured next for a 48 kHz sample rate. Finally, the digital mute is disabled to allow for audio playback.

The playback function performs the following procedure:

1. Set the channel’s prescale value to obtain the appropriate bit rate.
2. Set the channel’s word select values.
3. Fill the FIFO with data.
4. Clear the interrupt mask register.
5. Reset the interrupt sense register by writing ‘1’.
6. Enable data transfer by writing a ‘1’ to the enable bit in the control register.
7. Wait for the FIFO almost empty interrupt to occur.
8. Repeat from step 3.

# The record function performs the same procedure with a different FIFO interaction:

1. Set the channel’s prescale value to obtain the appropriate bit rate.
2. Set the channel’s word select values.
3. Clear the interrupt mask register.
4. Reset the interrupt sense register by writing ‘1’.
5. Enable data transfer by writing a ‘1’ to the enable bit in the control register.
6. Wait for the FIFO almost full interrupt to occur.
7. Read from the FIFO.
8. Repeat from step 3.

The basic system is implemented using busy waiting for the button presses and the interrupt status.

# Next Stage

First, the basic system will be refined by adding edge triggered interrupts to the buttons used to initiate audio recording and playback, and to the detection of the LOGII2S interrupt. Following this, the features of the advanced system will be implemented. An additional IP for computing FFTs will be added, and ethernet will be enabled for data streaming to the host.

# Conclusion

A basic audio recorder was built on the Zybo board using a new I2S IP (Xylon’s LogicBricks LOGII2S). The advanced system will additional data processing and data streaming via ethernet.